

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,830,964 B1
 APPLICATION NO. : 10/647061
 DATED : December 14, 2004
 INVENTOR(S) : Robert J. Mears et al.

Page 1 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page should be deleted to appear as per attached title page.

The sheet of drawing consisting of figure 1 should be deleted to appear as per attached figure 1.

Column 1, Line 44 Delete: "on a binary"
 Insert: --on binary--

Column 2, Line 2 Delete: "in a silicon"
 Insert: --in silicon--

Column 2, Line 3 Delete: "electromuminescence"
 Insert: --electroluminescence--

Column 2, Line 62 Delete: "superlattice and has"
 Insert: --superlattice has--

Column 3, Line 49 Delete: "Si/o"
 Insert: --Si/O--

Column 4, Line 32 Delete:

$$\mathbf{M}_{k,ij}^{-1}(E_F, T) = \frac{- \sum_{E < E_F \text{ B.Z.}} \int (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_i (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_j \frac{\partial f(E(\mathbf{k}, n), E_F, T)}{\partial E} d^3 \mathbf{k}''}{\sum_{E < E_F \text{ B.Z.}} \int (1 - f(E(\mathbf{k}, n), E_F, T)) d^3 \mathbf{k}}$$

Insert:

$$\mathbf{M}_{h,ij}^{-1}(E_F, T) = \frac{- \sum_{E < E_F \text{ B.Z.}} \int (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_i (\nabla_{\mathbf{k}} E(\mathbf{k}, n))_j \frac{\partial f(E(\mathbf{k}, n), E_F, T)}{\partial E} d^3 \mathbf{k}''}{\sum_{E < E_F \text{ B.Z.}} \int (1 - f(E(\mathbf{k}, n), E_F, T)) d^3 \mathbf{k}}$$

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Column 5, Line 13

Delete: "gate 35"
Insert: --gate 38--

Column 5, Line 61

Delete: "gate 35"
Insert: --gate 38--

Column 7, Line 63

Delete: "from the both"
Insert: --from both--

Column 9, Lines
44-46

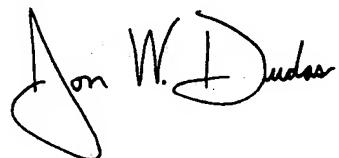
Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."

Column 9, Line 59

Delete: "also formed"
Insert: --also be formed--

Signed and Sealed this

Twenty-fifth Day of September, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) United States Patent
Mears et al.(16) Patent No.: US 6,830,964 B1
(45) Date of Patent: Dec. 14, 2004

(54) METHOD FOR MAKING SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/647,061

(22) Filed: Aug. 22, 2003

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/603,695, filed on Jun. 26, 2003, and a continuation-in-part of application No. 10/603,621, filed on Jun. 26, 2003.

(51) Int. Cl.⁷ H01L 21/20

(52) U.S. Cl. 438/162; 438/479; 438/301

(58) Field of Search 438/149, 151-514, 438/162, 217, 222-228, 299-301, 479-508

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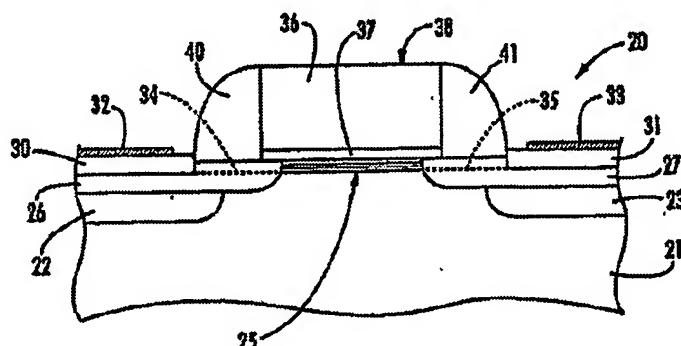
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(57) ABSTRACT

A method is for making a semiconductor device by forming a superlattice that, in turn, includes a plurality of stacked groups of layers. The method may also include forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers. Each group of the superlattice may include a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. The energy-band modifying layer may include at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice may have a higher charge carrier mobility in the parallel direction than would otherwise occur. The superlattice may also have a common energy band structure therein.

76 Claims, 9 Drawing Sheets



U.S. Patent

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